**Digital System design Processing Lab**

Assignment: 01



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TASK#1 **AND**

CODE

// Code your design here

module myand (a,b,y);

input a,b;

output y;

assign y = a&b; //dataflow

endmodule

**// Code your testbench here**

// or browse Examples

module myand\_tb;

reg a1,b1;

wire y1;

myand myand\_tb(.a(a1),.b(b1),.y(y1));

initial begin

$dumpfile("dump.vcd");

$dumpvars(1);

// $monitor(a1,b1,y1);

a1=1'b0;

b1=1'b0;

#1 $display("a1:%b, b1:%b, y1:%b",a1,b1,y1);

#1

a1=1'b0;

b1=1'b1;

#1 $display("a1:%b, b1:%b, y1:%b",a1,b1,y1);

#1

a1=1'b1;

b1=1'b0;

#1 $display("a1:%b, b1:%b, y1:%b",a1,b1,y1);

#1

a1=1'b1;

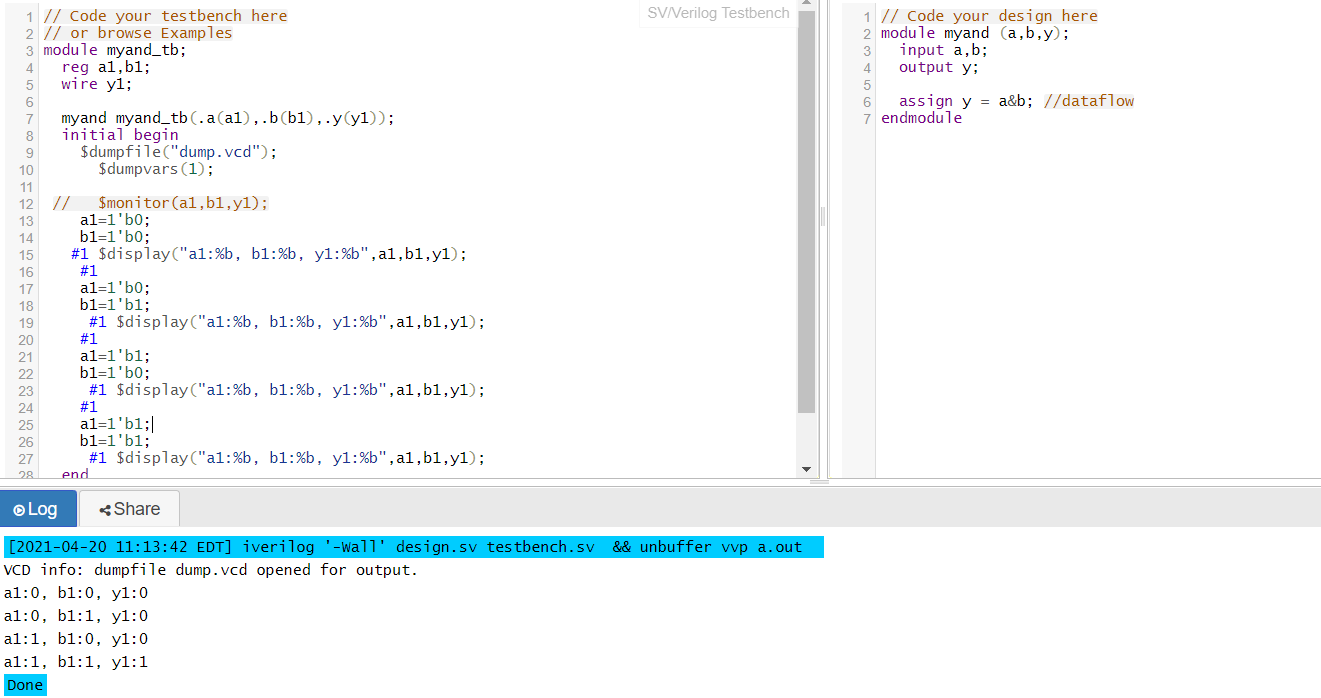
b1=1'b1;

#1 $display("a1:%b, b1:%b, y1:%b",a1,b1,y1);

end

endmodule

OUTPUT:



TASK 2: OR

CODE:

// Code your design here

module my (a,b,y);

input a,b;

output y;

assign y = a|b; //dataflow

endmodule

**// Code your testbench here**

// or browse Examples

module my\_tb;

reg a1,b1;

wire y1;

my my\_tb(.a(a1),.b(b1),.y(y1));

initial begin

$dumpfile("dump.vcd");

$dumpvars(1);

// $monitor(a1,b1,y1);

a1=1'b0;

b1=1'b0;

#1 $display("a1:%b, b1:%b, y1:%b",a1,b1,y1);

#1

a1=1'b0;

b1=1'b1;

#1 $display("a1:%b, b1:%b, y1:%b",a1,b1,y1);

#1

a1=1'b1;

b1=1'b0;

#1 $display("a1:%b, b1:%b, y1:%b",a1,b1,y1);

#1

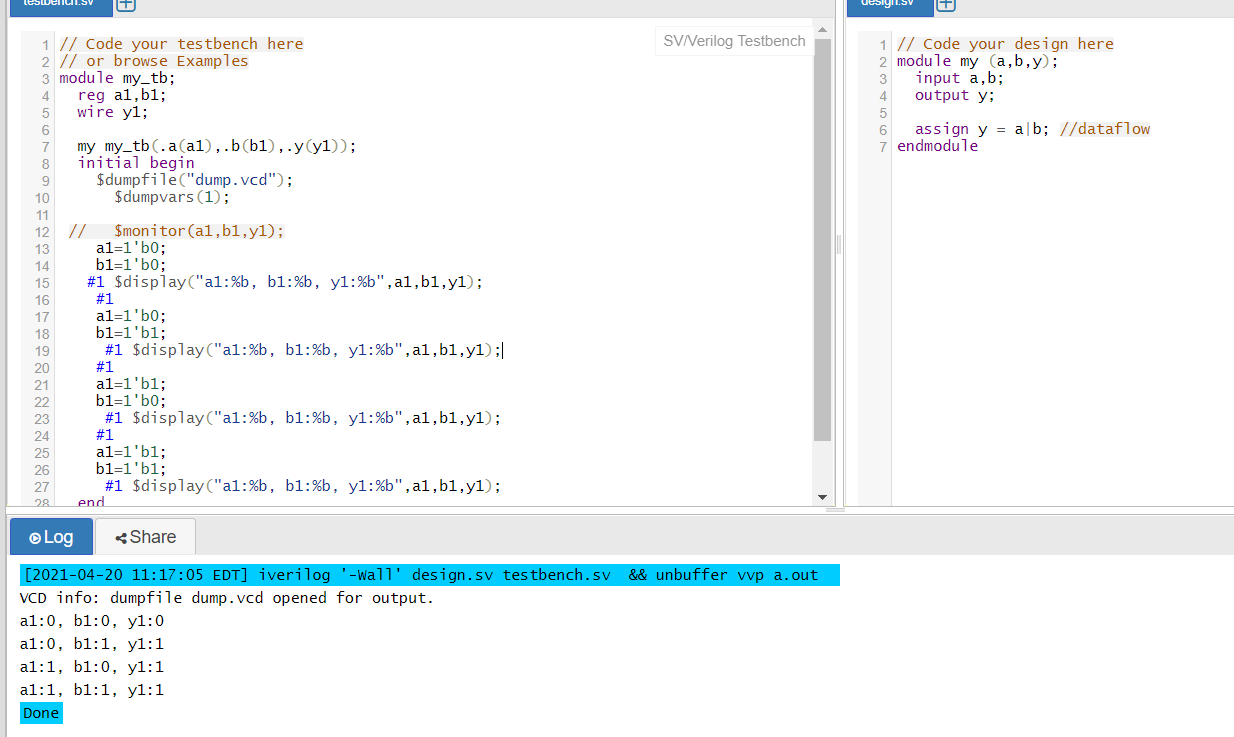
a1=1'b1;

b1=1'b1;

#1 $display("a1:%b, b1:%b, y1:%b",a1,b1,y1);

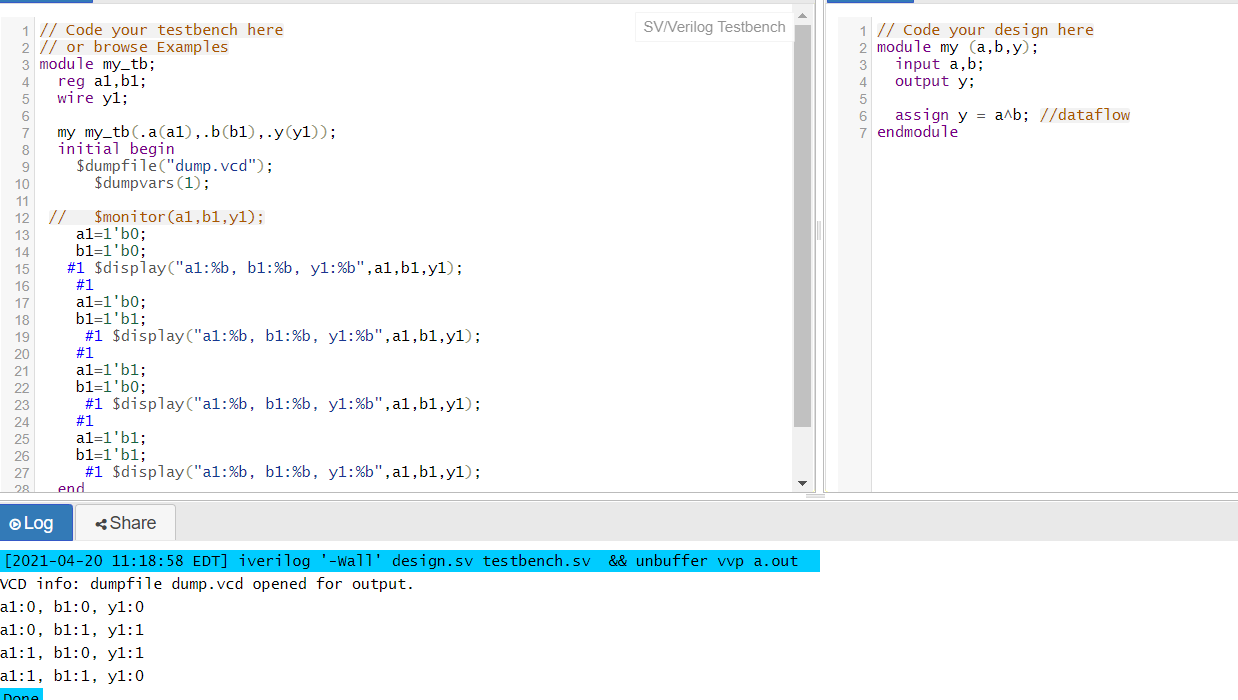
end

endmodule



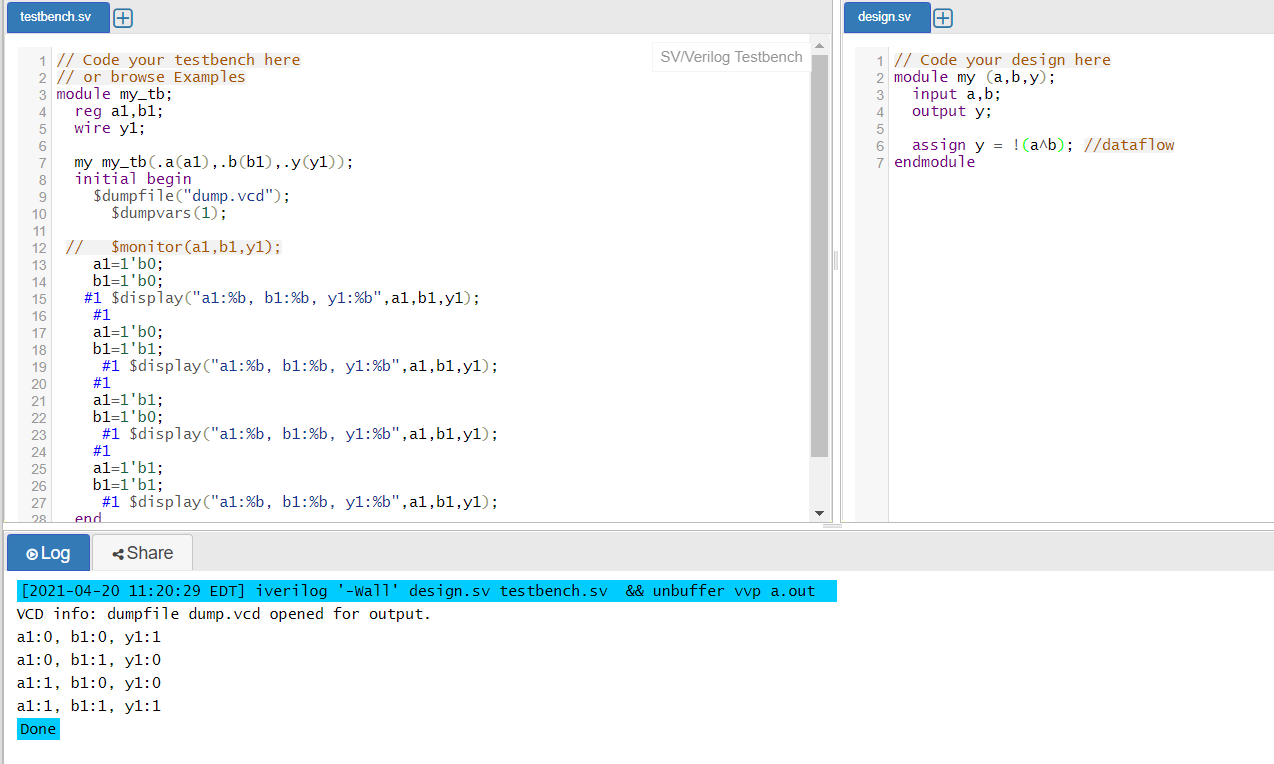
TASK 3: XOR

CODE:



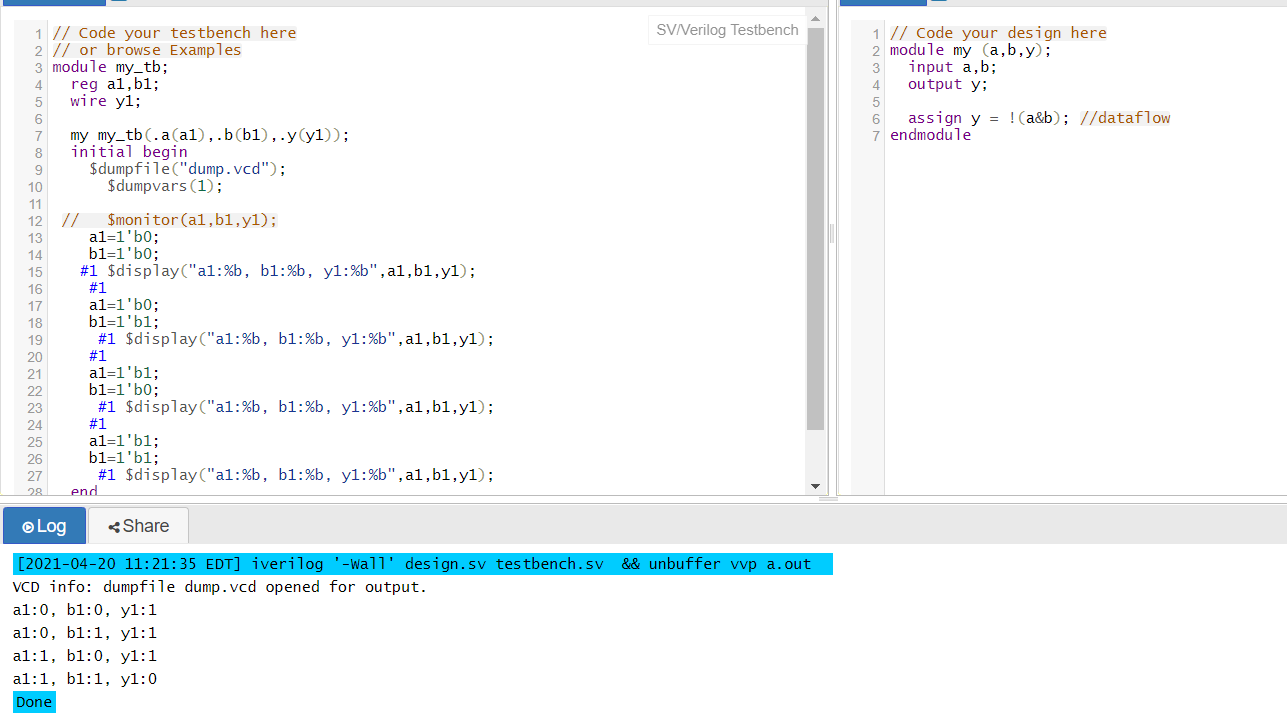
TASK 4: XNOR

CODE:



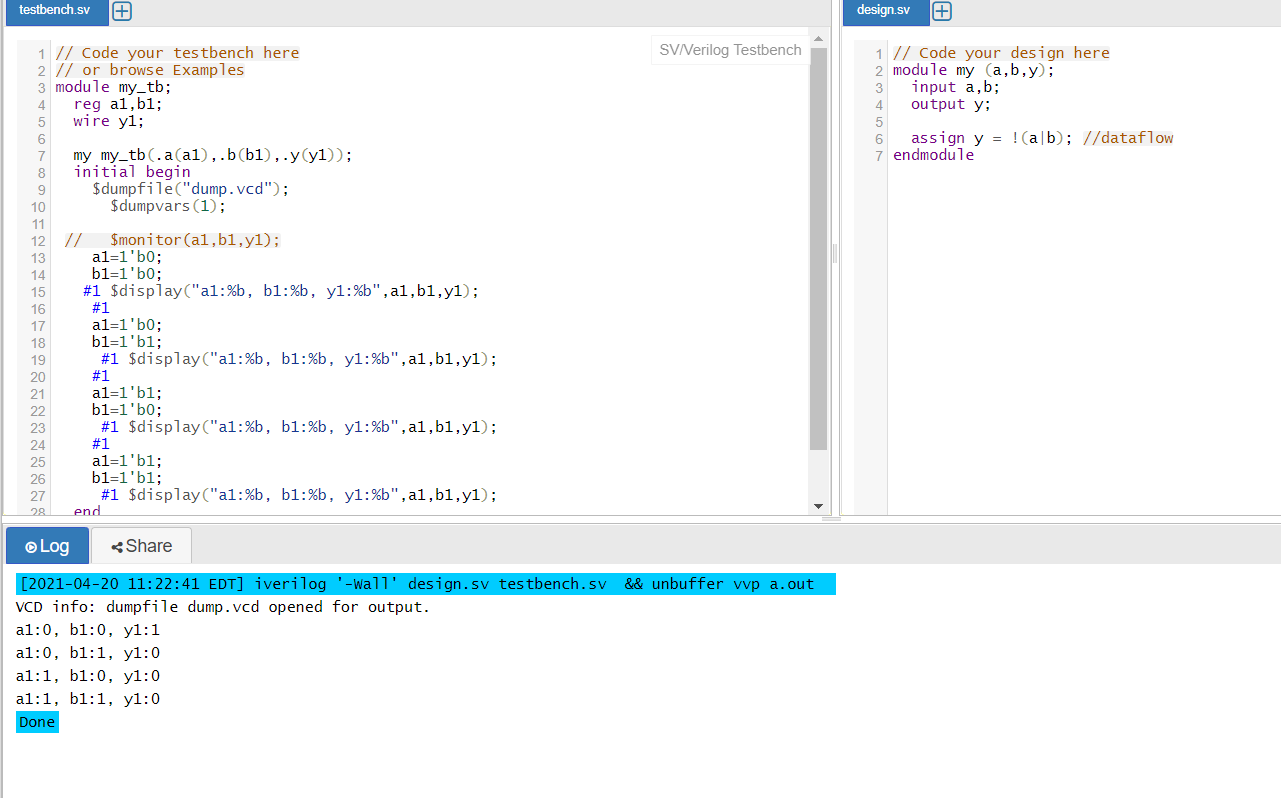
TASK 5: NAND

CODE:



TASK 5: NOR

CODE:



TASK 6:NOT GATE

CODE:

// Code your design here

module my (a,y);

input a;

output y;

assign y = ~a; //dataflow

endmodule

**// Code your testbench here**

// or browse Examples

module my\_tb;

reg a1;

wire y1;

my my\_tb(.a(a1),.y(y1));

initial begin

$dumpfile("dump.vcd");

$dumpvars(1);

$monitor(a1,y1);

a1=1'b0;

#1

a1=1'b1;

end

endmodule

